Amendments to the Claims

Please amend claims 1, 12, 23 and 29 as follows. This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Complete Listing of Claims:

1. (currently amended) A data processing system, comprising:

a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a ~~function~~ cycle;

a plurality of routing units, responsive to respective routing control signals, by which data is steered among inputs and outputs of the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different than another of said respective subsets; and

control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units to establish a route for a ~~function~~ cycle, where the route includes applying data output in the ~~function~~ cycle by a first functional unit in the plurality of functional units as input in the ~~function~~ cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the ~~function~~ cycle as input in the ~~function~~ cycle to a third functional unit in the ~~function~~ cycle.

2. (original) The data processing system of claim 1, wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

3. (original) The data processing system of claim 1, wherein said plurality of routing units includes at least one crossbar switch.

4. (original) The data processing system of claim 1, wherein said plurality of functional units includes at least one storage element.

5. (previously presented) The data processing system of claim 1, wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal.

6. (previously presented) The data processing system of claim 1, wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the control word distribution circuitry supplies at least one of the write control signals and read control signals.

7. (previously presented) The data processing system of claim 6, wherein the control word distribution circuitry supplies an address for said memory.

8. (original) The data processing system of claim 6, wherein an address for said memory is supplied by one of the plurality of functional units.

9. (original) The data processing system of claim 1, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

10. (original) The data processing system of claim 1, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

11. (previously presented) The data processing system of claim 1, wherein said control word distribution circuitry supplies said routing control signals synchronously to the plurality of routing units.

12. (currently amended) A data processing system, comprising:

a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a ~~function~~ cycle;

a plurality of routing units, responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks, routing units in the plurality of routing units being coupled to respective subsets of processing blocks in the plurality of processing blocks, wherein at least one of said respective subsets of processing blocks is different than another of said respective subsets processing blocks; and

block level control word distribution circuitry which supplies control words for respective ~~function~~ cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units; wherein processing blocks in said plurality of processing blocks respectively include

a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a block ~~function~~ cycle;

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units, unit level routing units in the plurality of unit level routing units being coupled to respective subsets of functional units in the plurality of functional unit, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units; and

functional unit level control word distribution circuitry which supplies control words for respective block ~~function~~ cycles to the plurality of unit level routing units, said control words including the routing control signals to establish a route in the block ~~function~~ cycle for the plurality of unit level routing units, where the route includes applying data output in the block ~~function~~ cycle by a first functional unit in the plurality of functional units as input in the block ~~function~~ cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the block ~~function~~ cycle as input in the block ~~function~~ cycle to a third functional unit in the block ~~function~~ cycle.

13. (original) The data processing system of claim 12, wherein said plurality of unit level routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

14. (original) The data processing system of claim 12, wherein said plurality of block level routing units includes at least one crossbar switch.

15. (original) The data processing system of claim 12, wherein said plurality of functional units includes at least one storage element.

16. (original) The data processing system of claim 12, wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control word.

17. (previously presented) The data processing system of claim 12, wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the function unit level control word distribution circuitry supplies includes at least one of the write control signals and read control signals.

18. (previously presented) The data processing system of claim 17, wherein said function unit level control word distribution circuitry supplies includes an address for said memory.

19. (original) The data processing system of claim 17, wherein an address for said memory is supplied by one of the plurality of functional units.

20. (original) The data processing system of claim 12, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

21. (original) The data processing system of claim 12, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

22. (previously presented) The data processing system of claim 12, wherein at least one of said block level control word distribution circuitry and functional level control word distribution circuitry supplies said control words synchronously.

23. (currently amended) A method of processing data, in a data processing engine that includes a plurality of functional units, comprising:

providing a set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a route for a ~~function~~ cycle among the plurality of functional units; and

routing data among the plurality of functional units according to the set of software routing control signals and performing tasks in the plurality of functional units using the route to produce a result, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the route includes applying data output in the ~~function~~ cycle by a first functional unit in the plurality of functional units as input in the ~~function~~ cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the ~~function~~ cycle as input in the ~~function~~ cycle to a third functional unit in the ~~block function~~ cycle.

24. (previously presented) The method of claim 23, including:

compiling a high level programming language specifying the result to produce the set of software routing control signals.

25. (previously presented) The method of claim 23, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

26. (previously presented) The method of claim 23, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

27. (previously presented) The method of claim 23, wherein the routing units in the data processing engine comprise a plurality of switches interconnecting the plurality of functional units, and said set of routing control signals specify data paths through the plurality of switches.

28. (original) The method of claim 23, including synchronously routing said data among the plurality of functional units.

29. (currently amended) A method of processing data in a data processing engine that includes a plurality of functional units, comprising;

providing a first set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a first data path according to a first configuration of the plurality of functional units for a first ~~function~~ cycle, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the first data path includes applying data output in the first ~~function~~ cycle by a first functional unit in the plurality of functional units as input in the first ~~function~~ cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the first ~~function~~ cycle as input in the first ~~function~~ cycle to a third functional unit in the first ~~block function~~ cycle;

performing tasks in said plurality of functional units using the first data path in the first ~~function~~ cycle;

providing a second set of software routing control signals in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units for a second ~~function~~ cycle, whereby the plurality of functional units is reconfigured to perform a different function; and

performing tasks in said plurality of functional units using the second data path to accomplish said different function in the second ~~function~~ cycle.

30. (original) The method of claim 29, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

31. (original) The method of claim 29, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

32. (previously presented) The method of claim 29, wherein the routing units in the data processing engine comprises a plurality of switches interconnecting the plurality of functional units, and said first and second sets of routing control signals specify data paths through the plurality of switches.

33. (previously presented) The method of claim 29, including:

compiling a high level programming language specifying the result to produce the first and second sets of software routing control signals.

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